IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/420,635
Filing Date ..... October 21, 1999
Inventor ..... Werner Juengling
Assignee ..... Micron Technology, Inc.
Group Art Unit 1746
Examiner ..... Unknown
Attorney's Docket No. MI22-1243
Title: Semiconductor Processing Methods of Forming Devices on a Substrate, Forming Device Arrays on a Substrate, Forming Conductive Lines on a Substrate, and Forming Capacitor Arrays on a Substrate, and Integrated Circuitry

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patent listed on the attached Form PTO-1449. No admission is made regarding whether the submitted reference is prior art.

This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing of a first Office Action, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. §1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Citation of these references is respectfully requested.

Respectfully submitted,

Date: Jan. 25, 2001

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138
Wells, St. John, Roberts, Gregory & Matkin P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828 (509) 624-4276